

FIG. 1

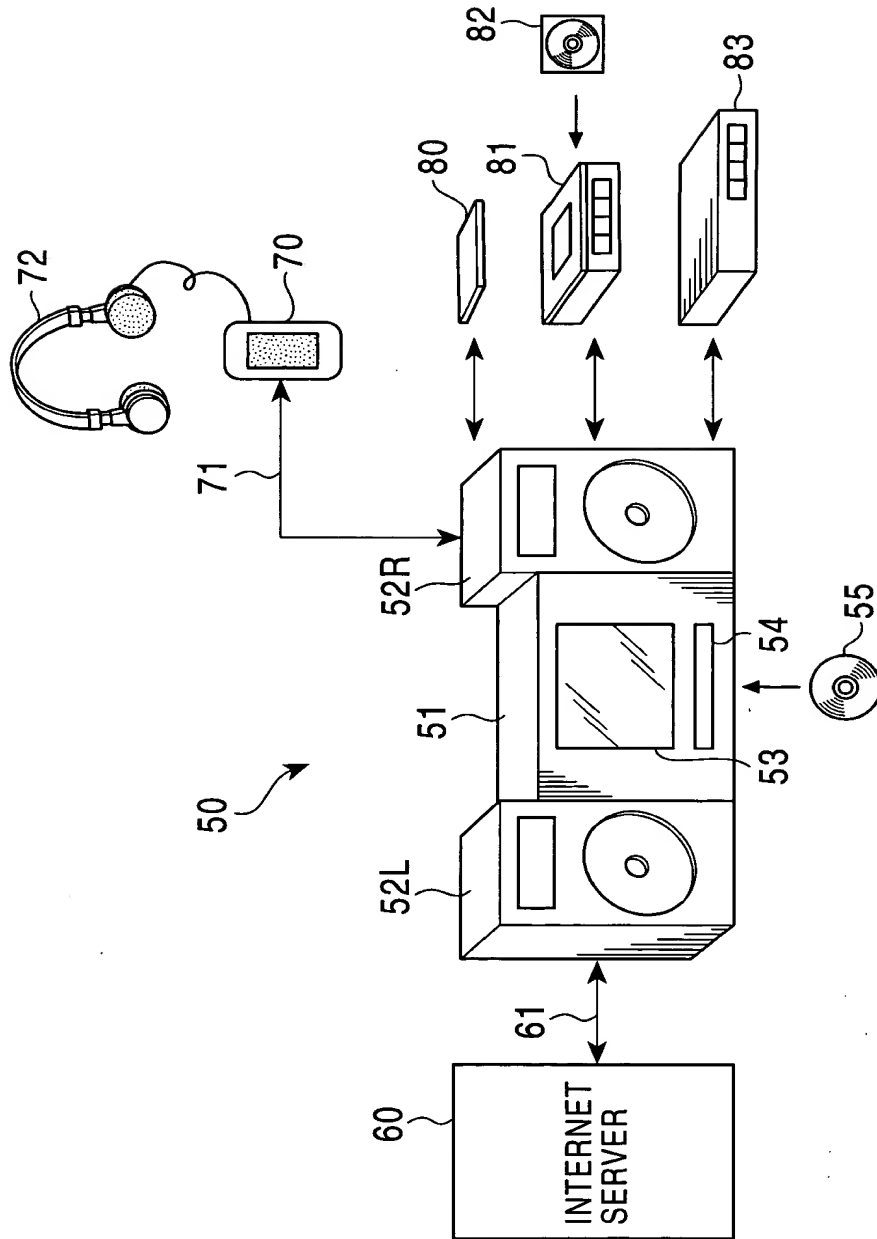


FIG. 2

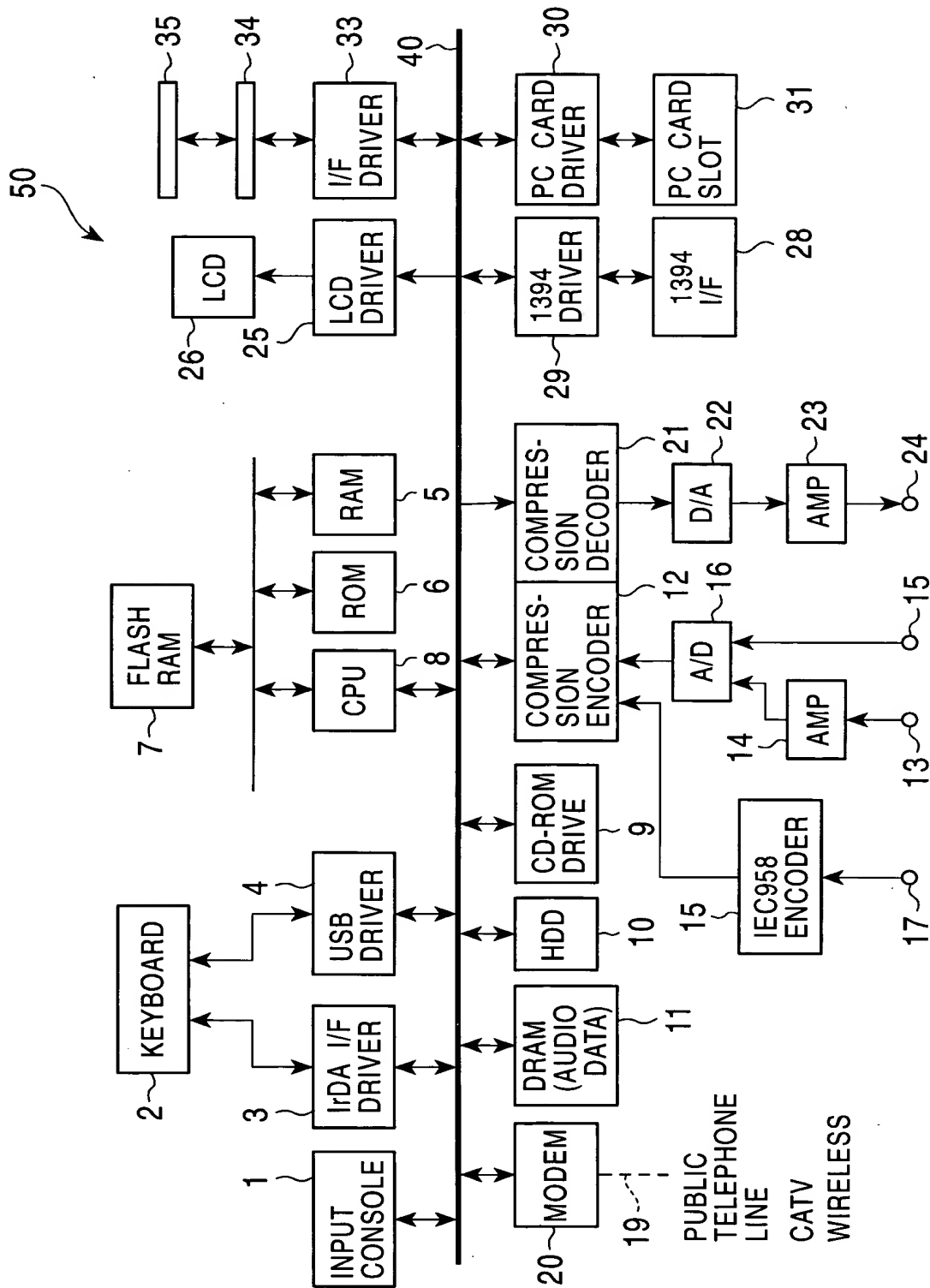


FIG. 3

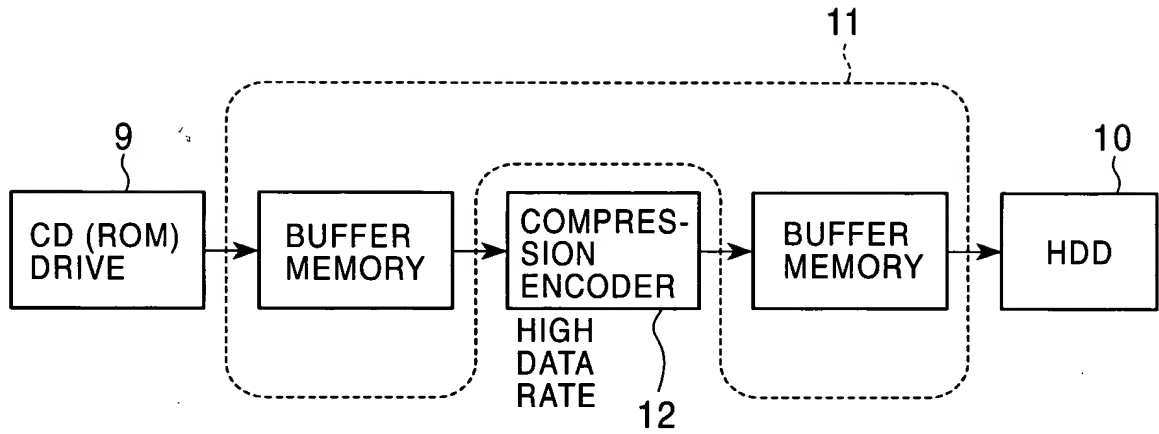
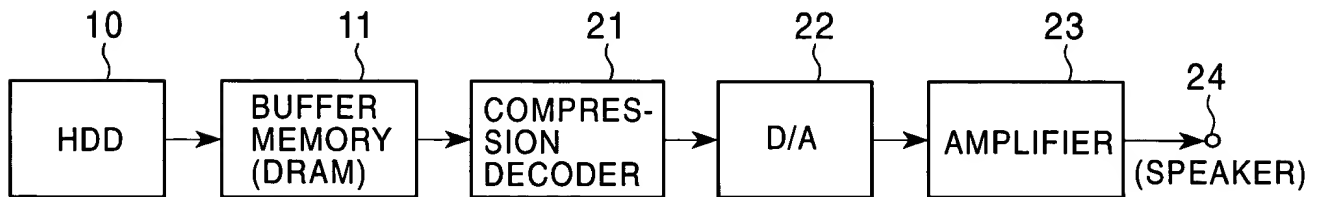


FIG. 4



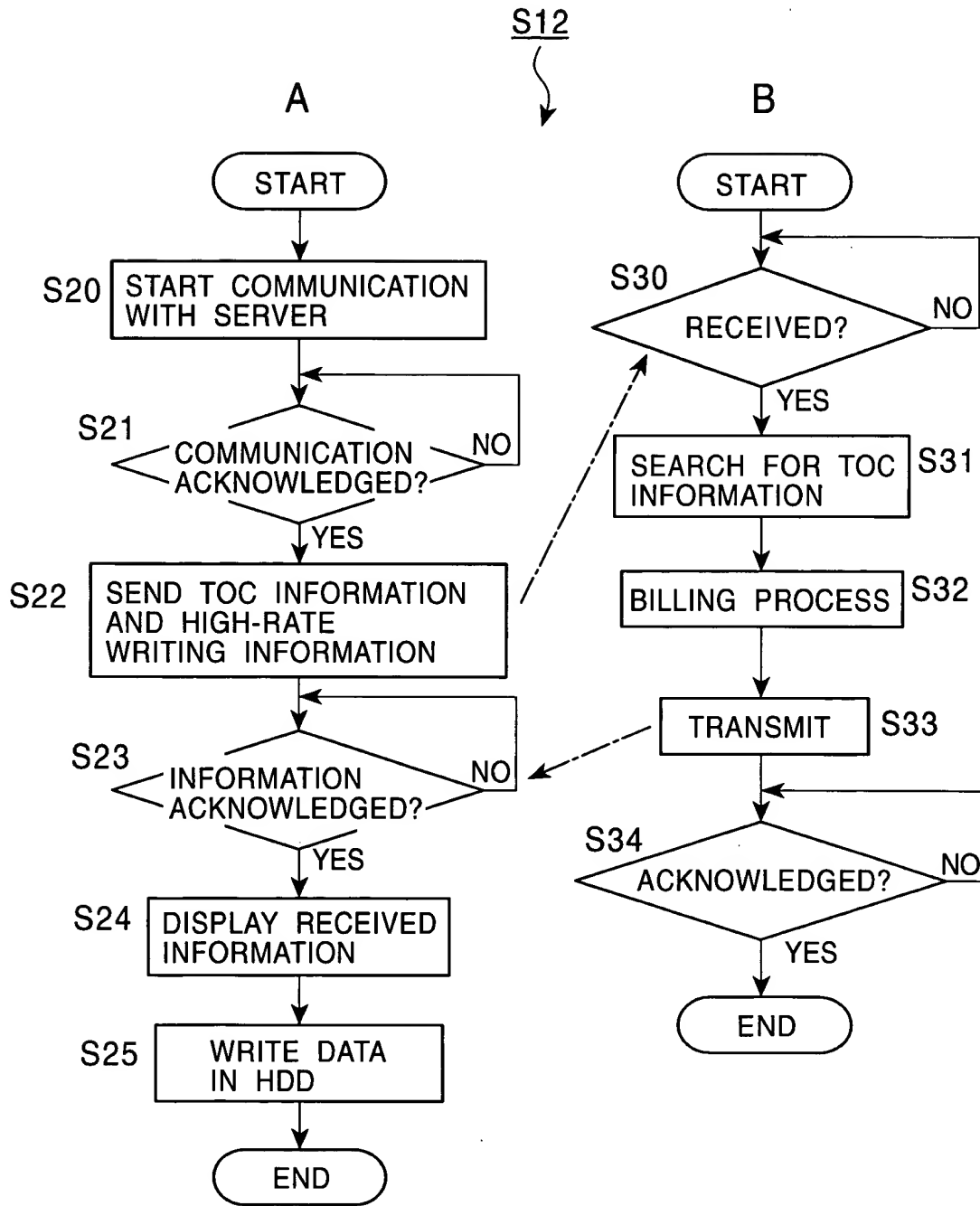
004201" 4.64660


```

graph TD
    START([START]) --> CD_HDD[CD → HDD  
WRITING  
REQUESTED?]
    CD_HDD -- NO --> START
    CD_HDD -- YES --> HIGH_RATE{HIGH RATE  
OR EQUI-RATE?}
    HIGH_RATE -- EQUI-RATE --> S14[S14  
START LOW-RATE  
COMPRESSION  
ENCODING]
    HIGH_RATE -- HIGH-RATE --> BILLING[START BILLING  
SYSTEM]
    BILLING --> HIGH_RATE_COMP[START HIGH-RATE  
COMPRESSION  
ENCODING]
    S14 --> DATA_TRANSFER[DATA FROM CD-ROM  
AND TRANSFER  
TO HDD]
    HIGH_RATE_COMP --> DATA_TRANSFER
    DATA_TRANSFER --> TRANSFER_ENDED{TRANSFER  
ENDED?}
    TRANSFER_ENDED -- NO --> CD_HDD
    TRANSFER_ENDED -- YES --> PROHIBIT[PROHIBIT CD →  
HDD TRANSFER]
    PROHIBIT --> LOW_RATE_COMP[START LOW-RATE  
COMPRESSION  
ENCODING]
    LOW_RATE_COMP --> END([END])

```

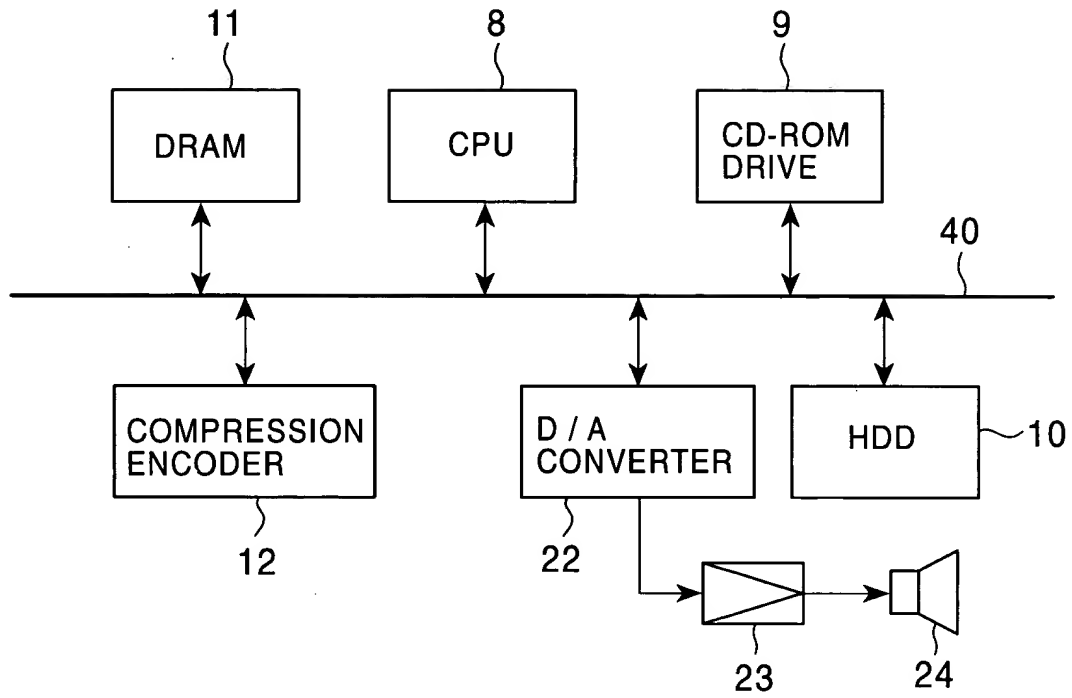
FIG. 8



START



FIG. 10



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FIG. 11

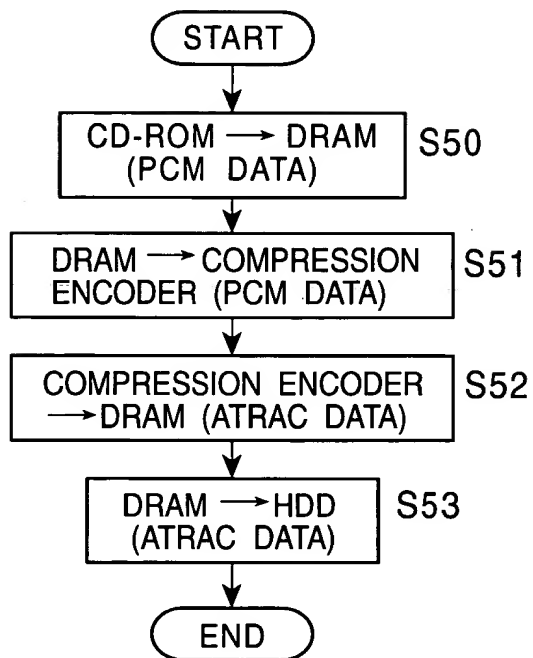


FIG. 12

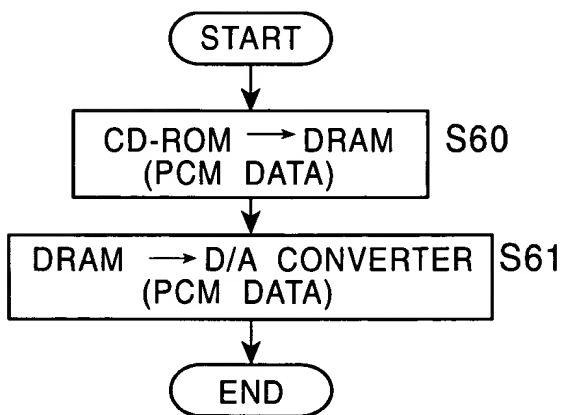


FIG. 13A

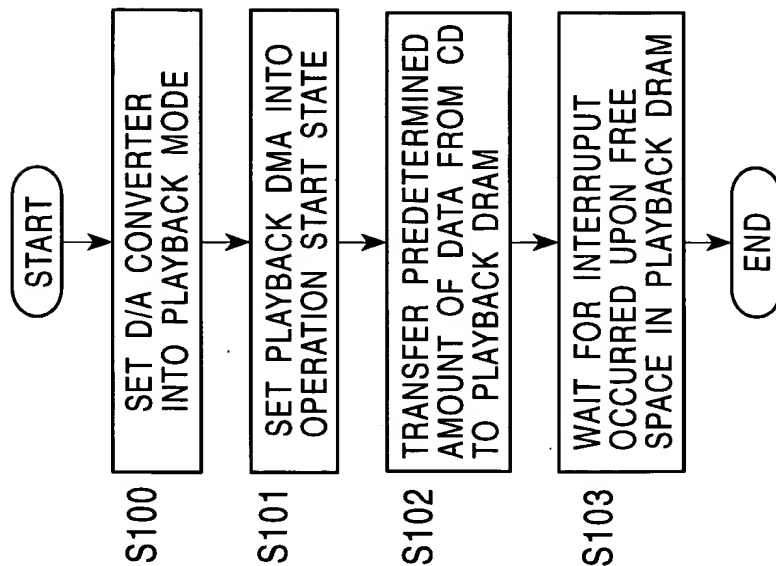


FIG. 13B

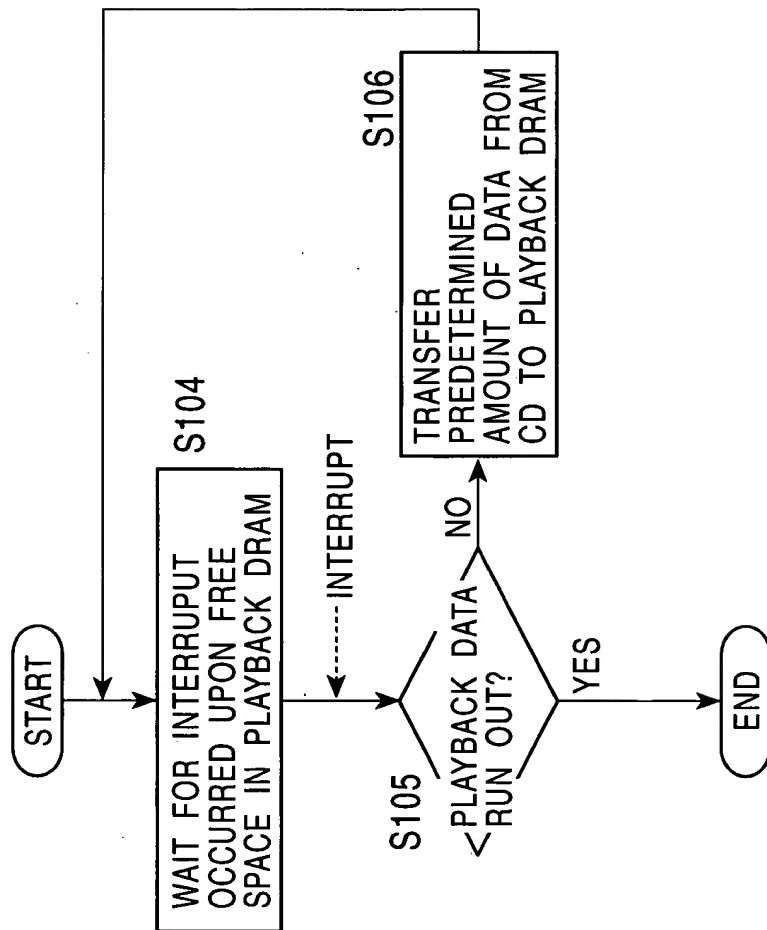


FIG. 14A

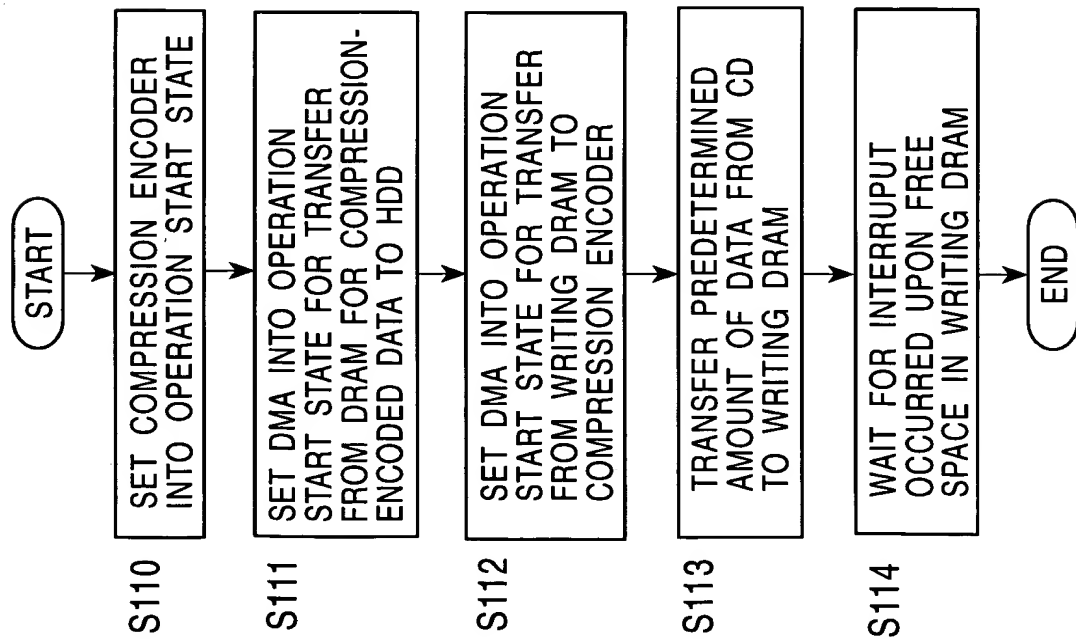


FIG. 14B

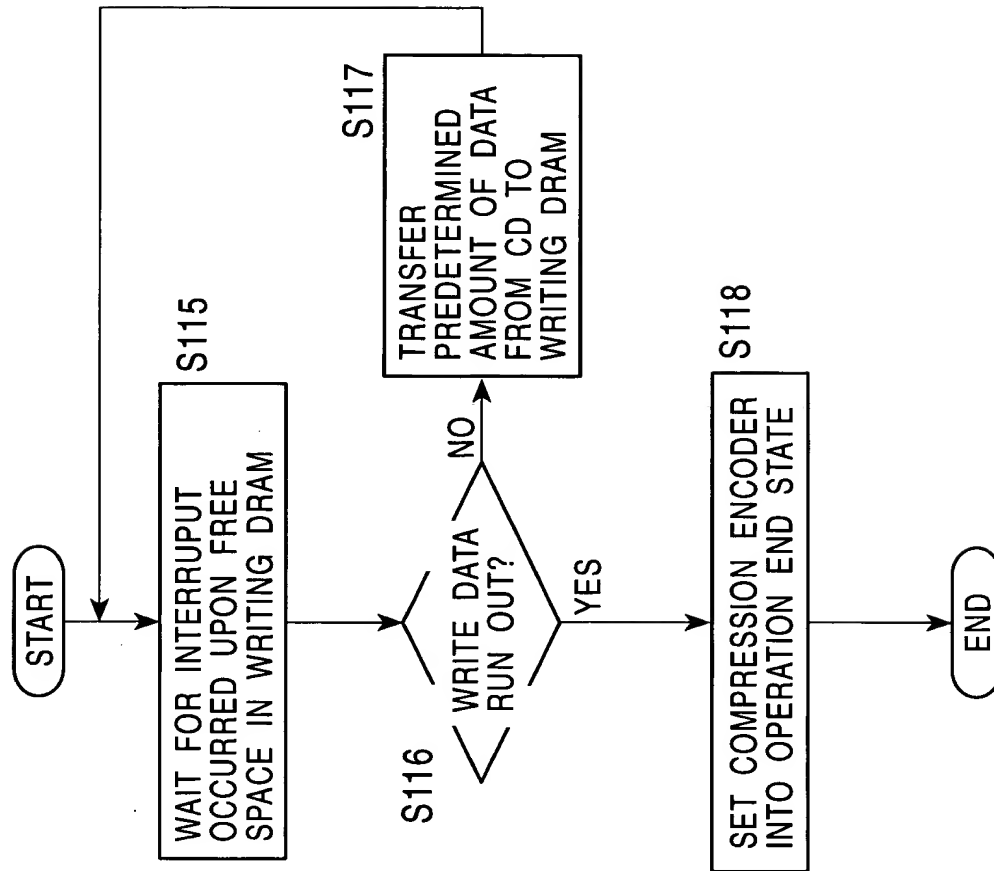


FIG. 15

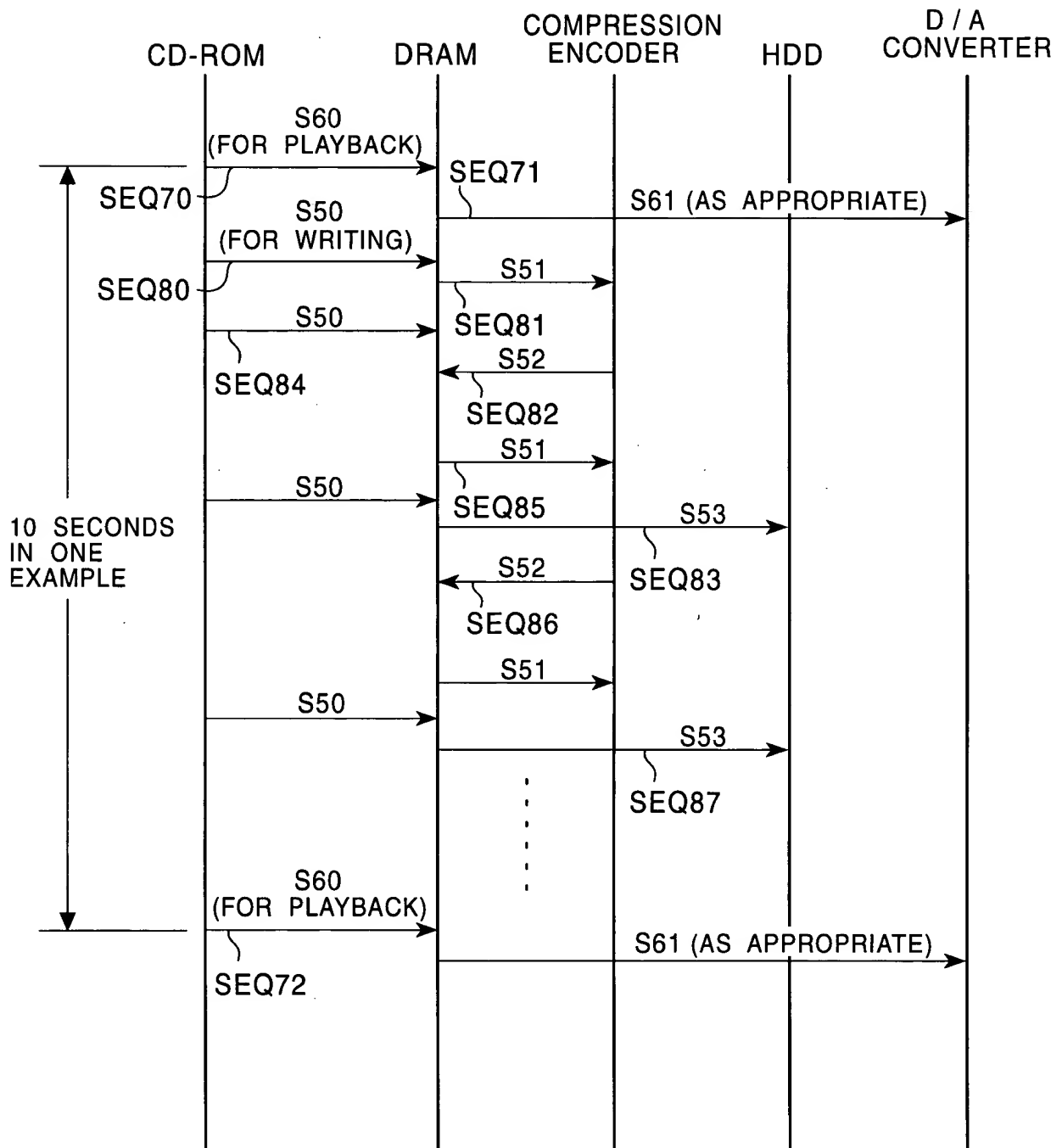


FIG. 16

DATA OF ONE PIECE OF MUSIC (52 SECONDS)

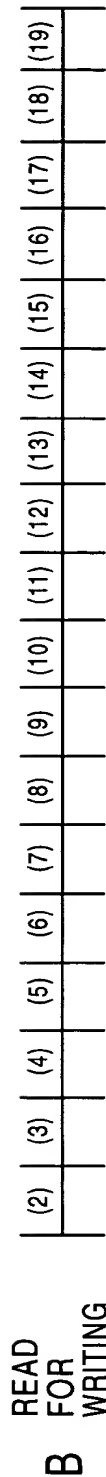
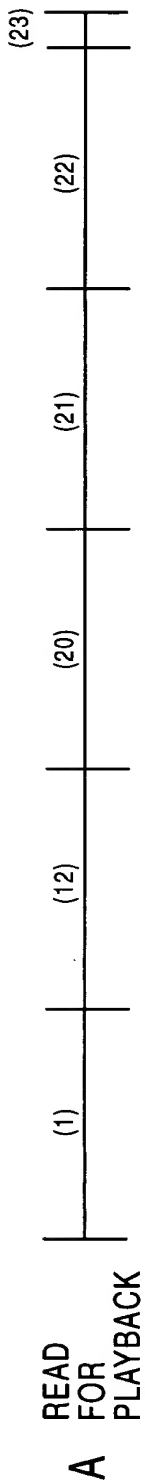
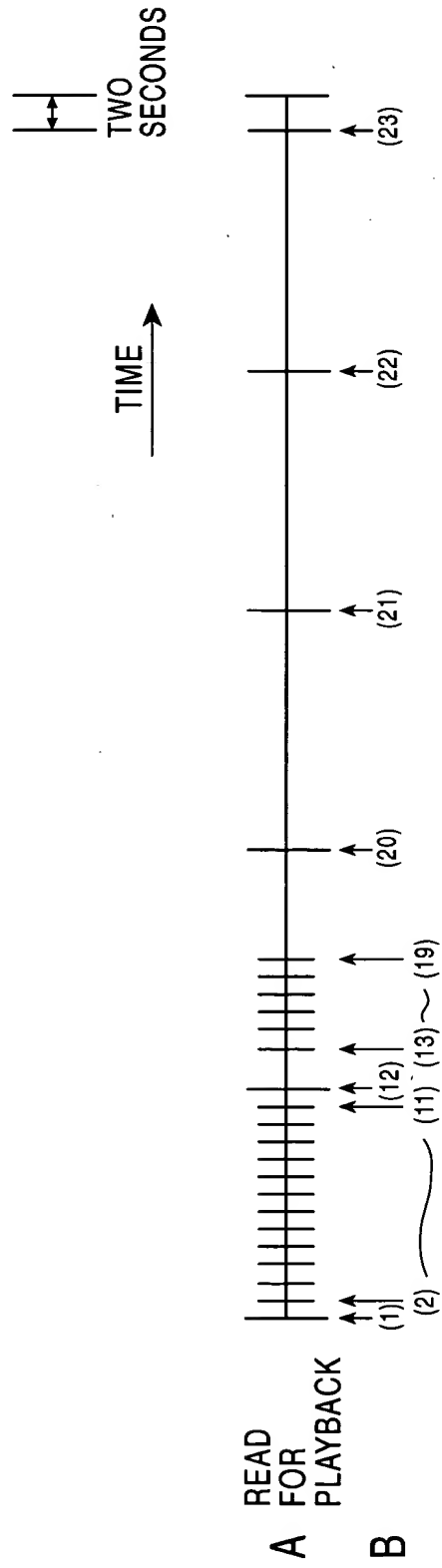


FIG. 17



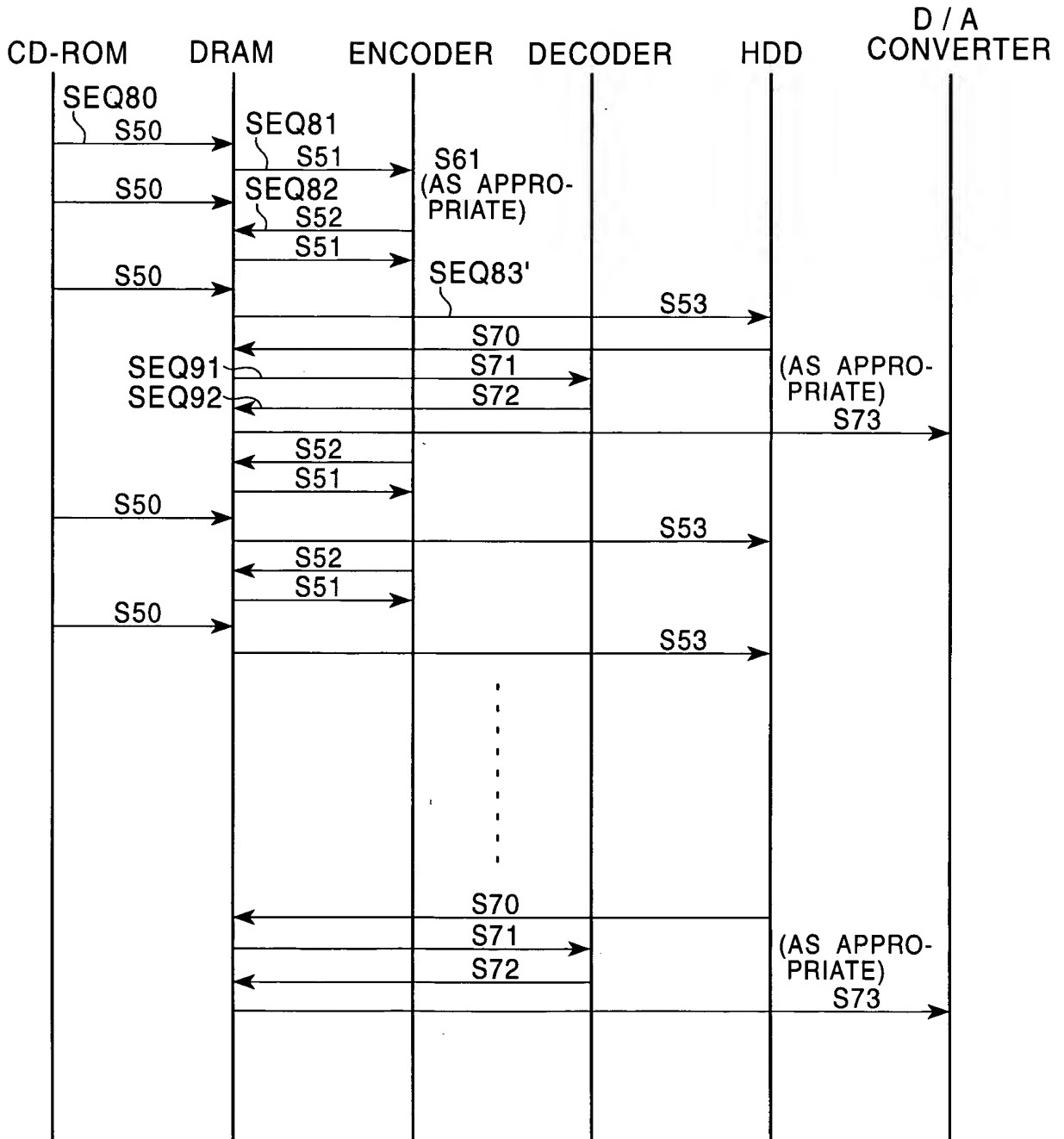
The diagram illustrates a computer system architecture. A central horizontal line represents a system bus, labeled 40. Above the bus are three components: DRAM (labeled 11), CPU (labeled 8), and CD-ROM DRIVE (labeled 9). Below the bus are four components: COMPRESSION ENCODER (labeled 12), COMPRESSION DECODER (labeled 21), D/A CONVERTER (labeled 22), and HDD (labeled 10). Bidirectional arrows connect each of these components to the bus. Additionally, a unidirectional arrow points from the D/A CONVERTER (22) to a speaker (labeled 24), with a small trapezoidal component (labeled 23) positioned between them.

```

graph TD
    START([START]) --> S70[HDD → DRAM  
(ATRAC DATA)]
    S70 --> S71[DRAM → COMPRESSION  
DECODER (ATRAC DATA)]
    S71 --> S72[COMPRESSION DECODER  
→ DRAM (PCM DATA)]
    S72 --> S73[DRAM → D/A CONVERTER  
(PCM DATA)]
    S73 --> END([END])

```

FIG. 20



BOOKS IN THE SERIES

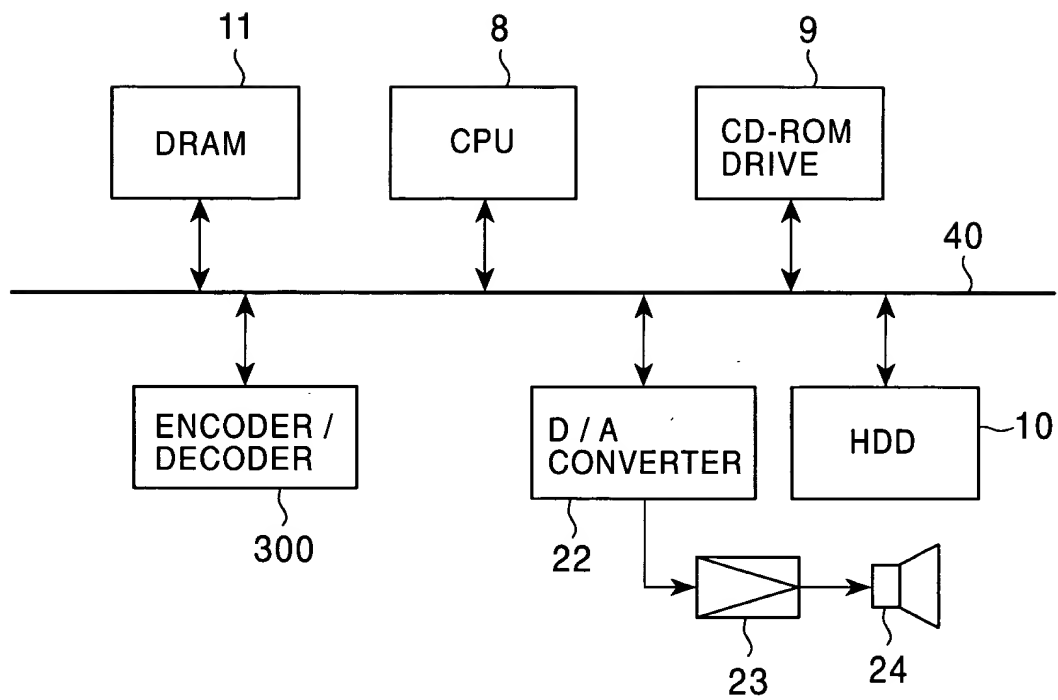


FIG. 22

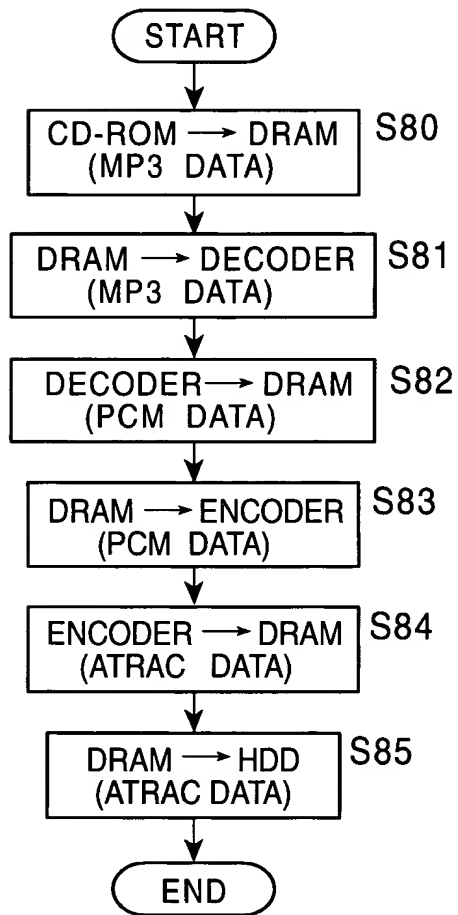


FIG. 23

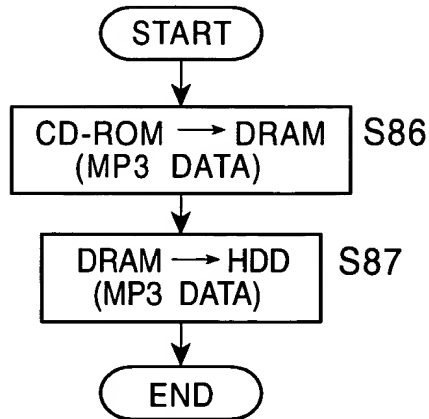
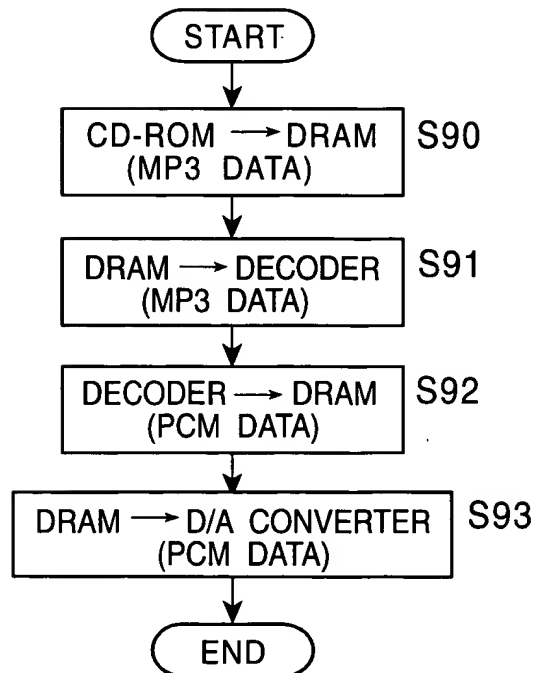


FIG. 24



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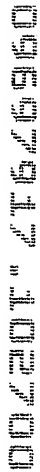


FIG. 26

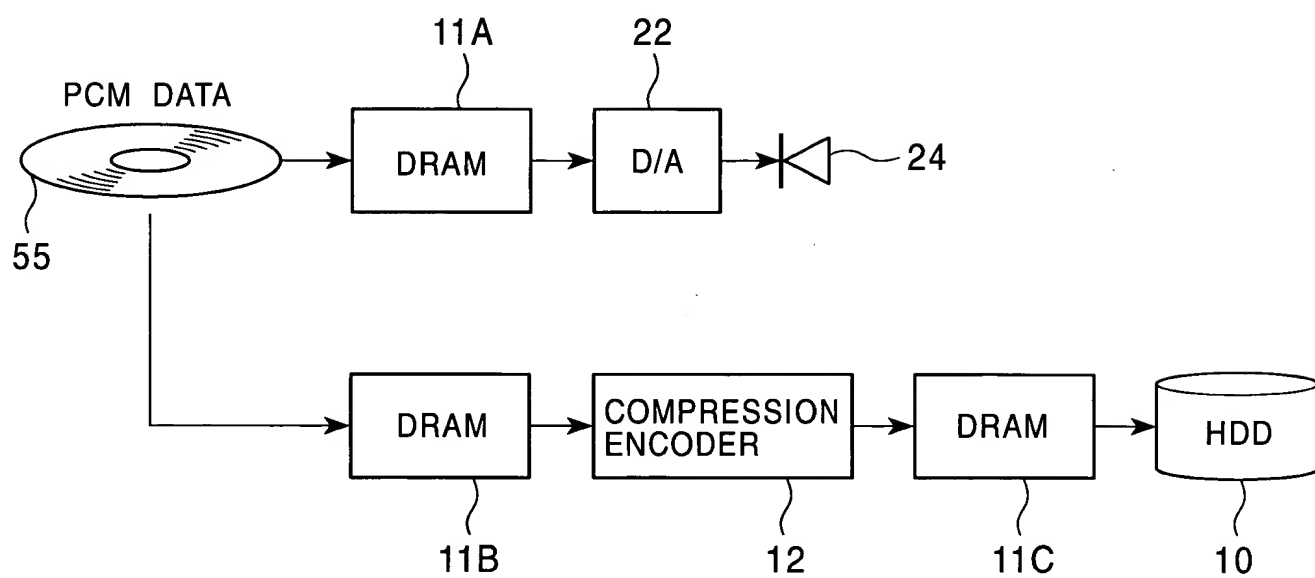


FIG. 27

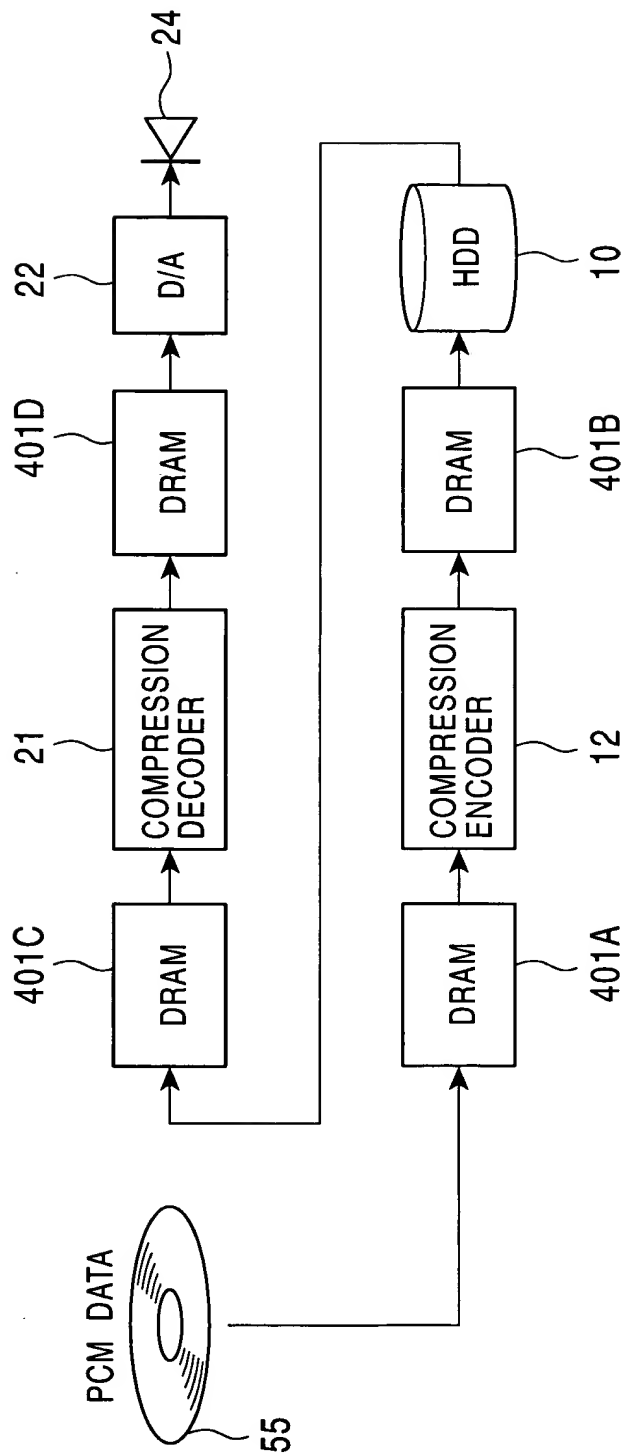


FIG. 28

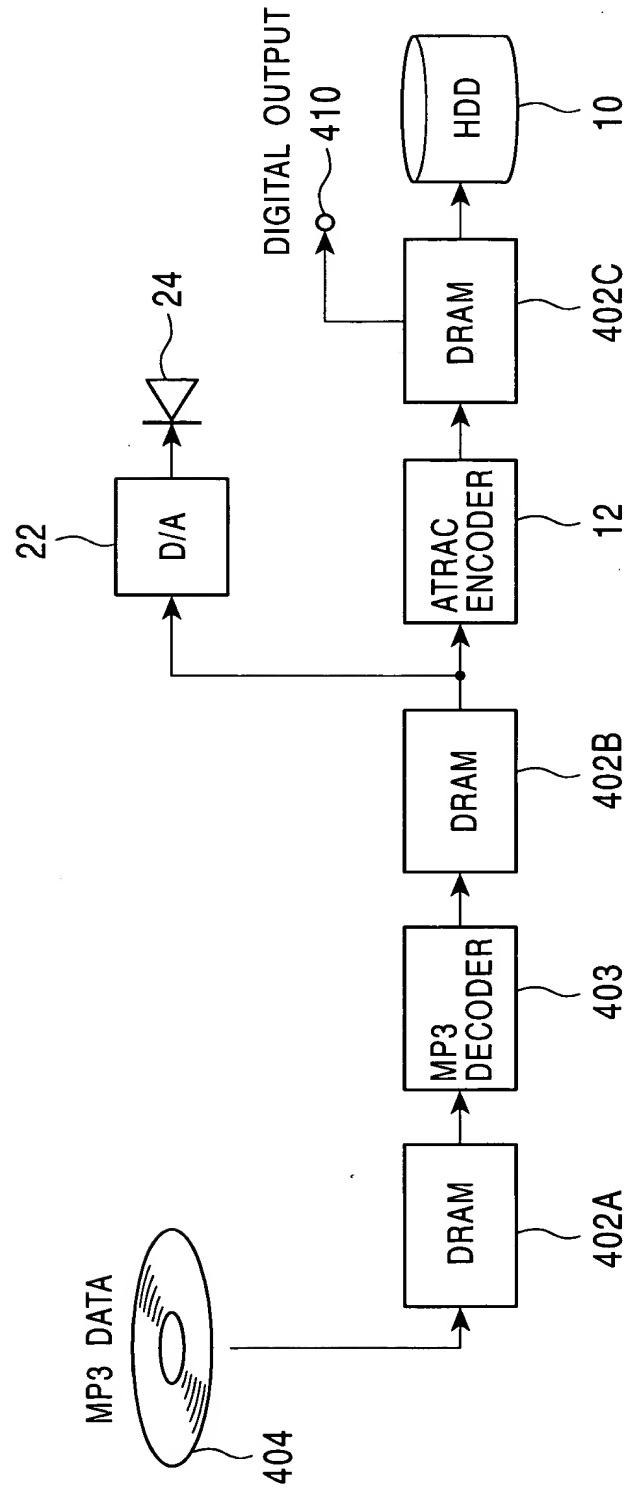


FIG. 29

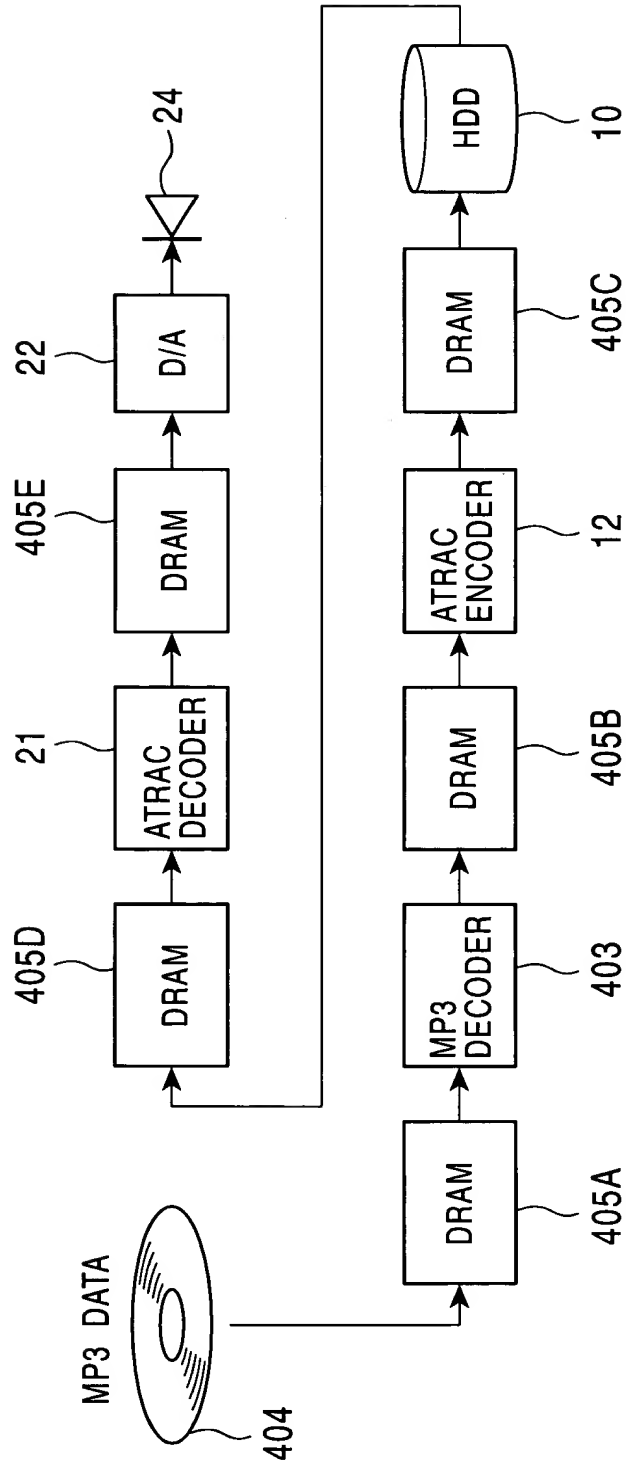


FIG. 30

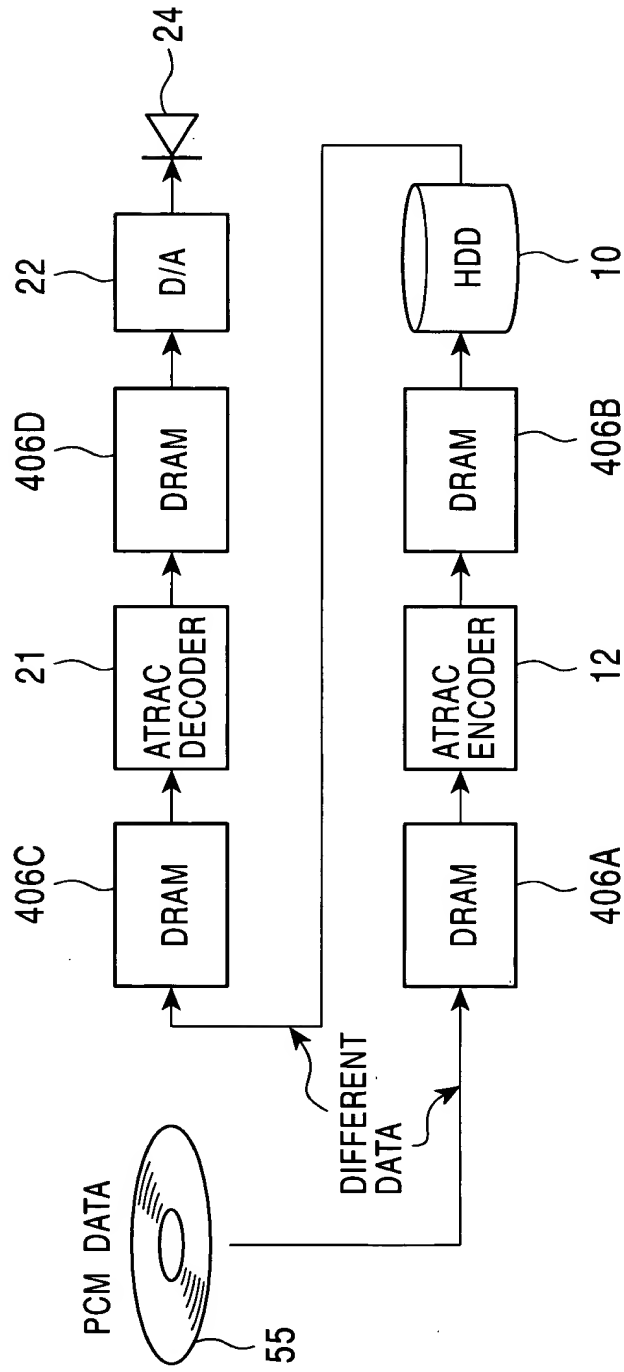


FIG. 31

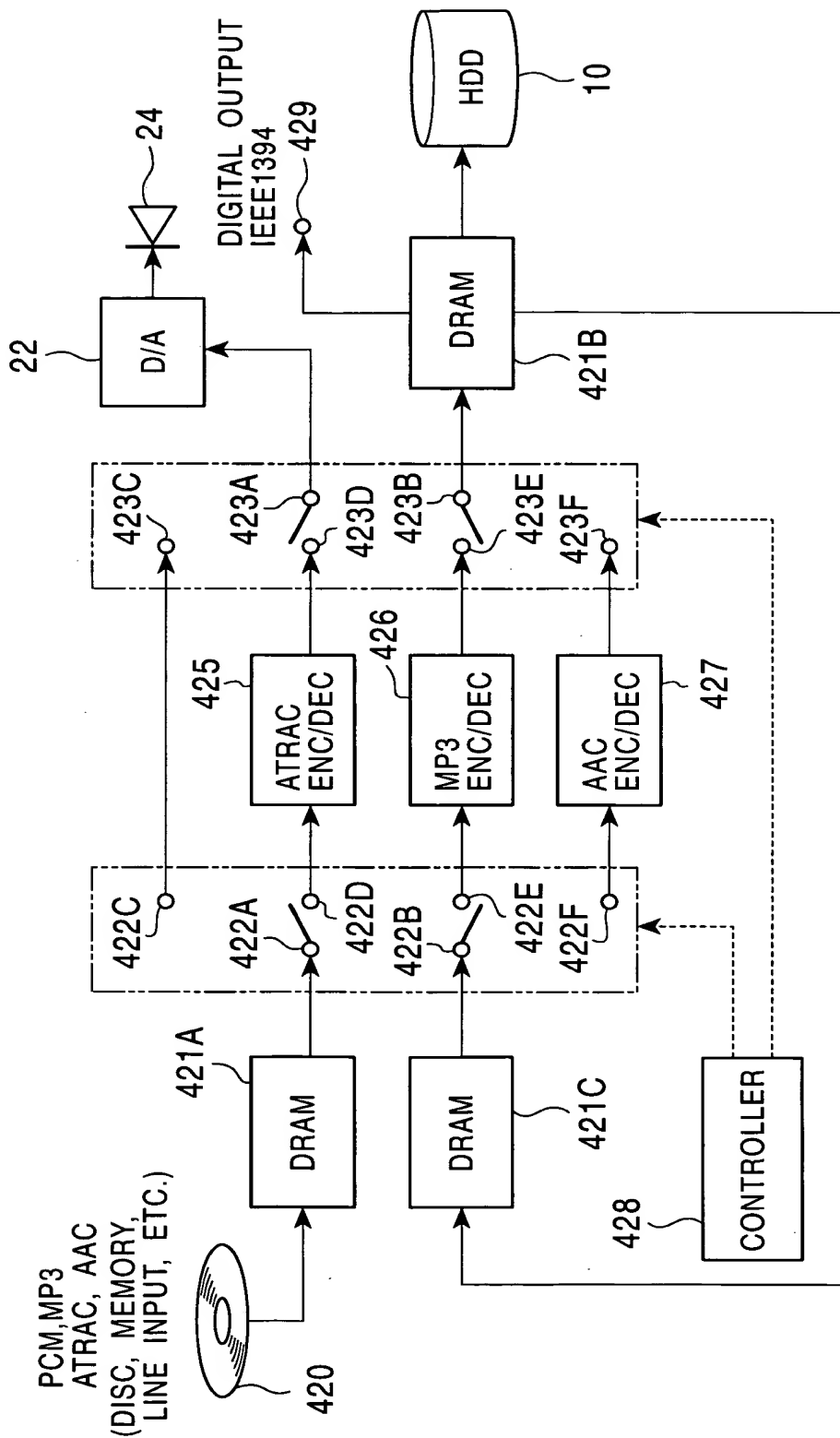
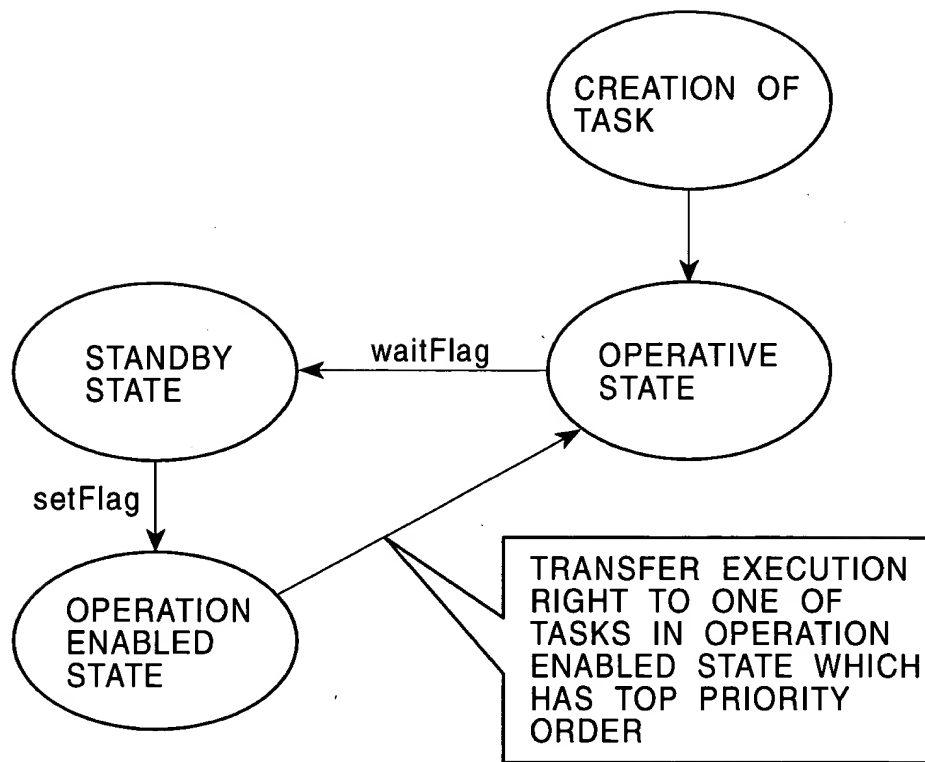


FIG. 32



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FIG. 33

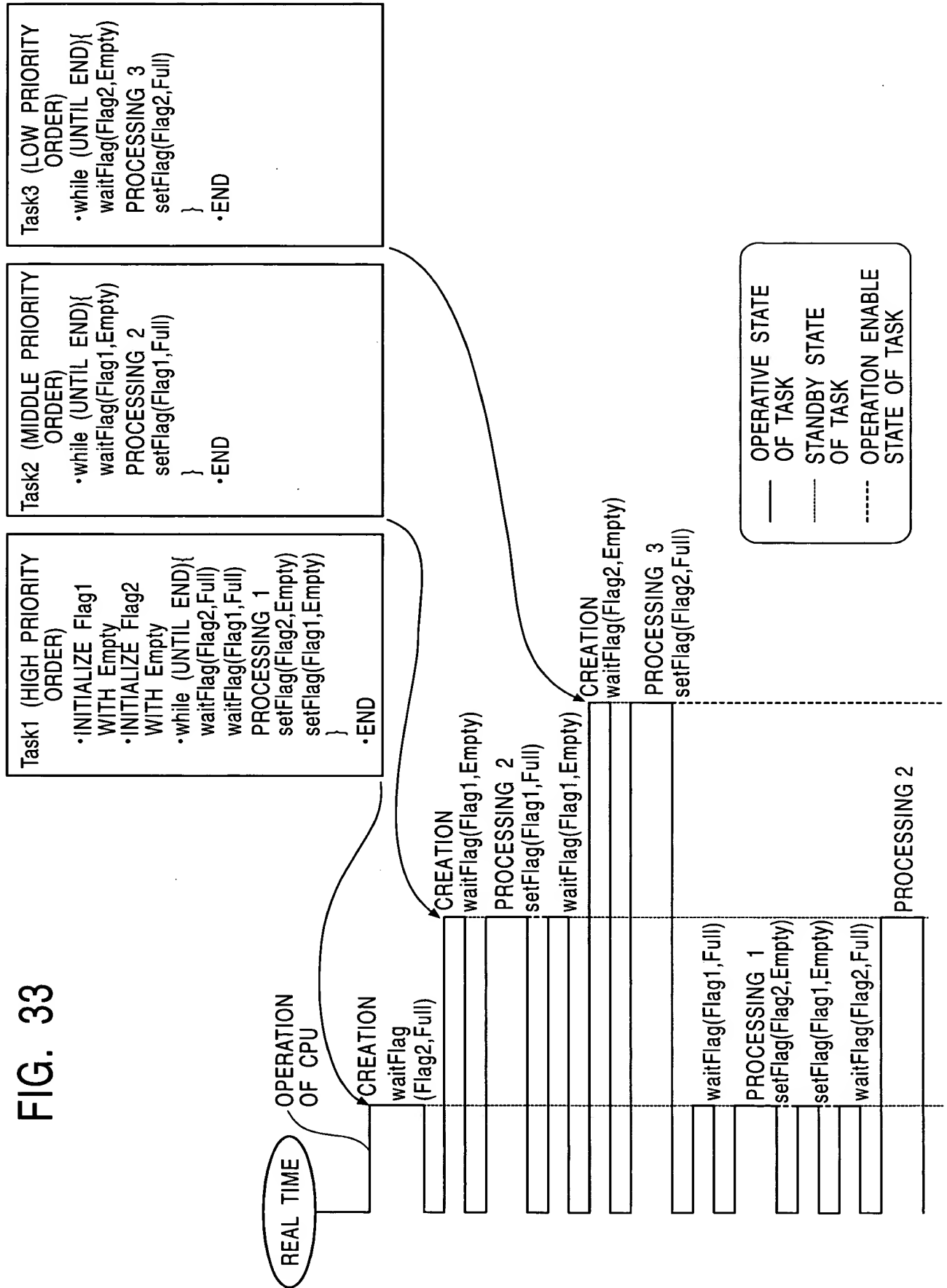


FIG. 34

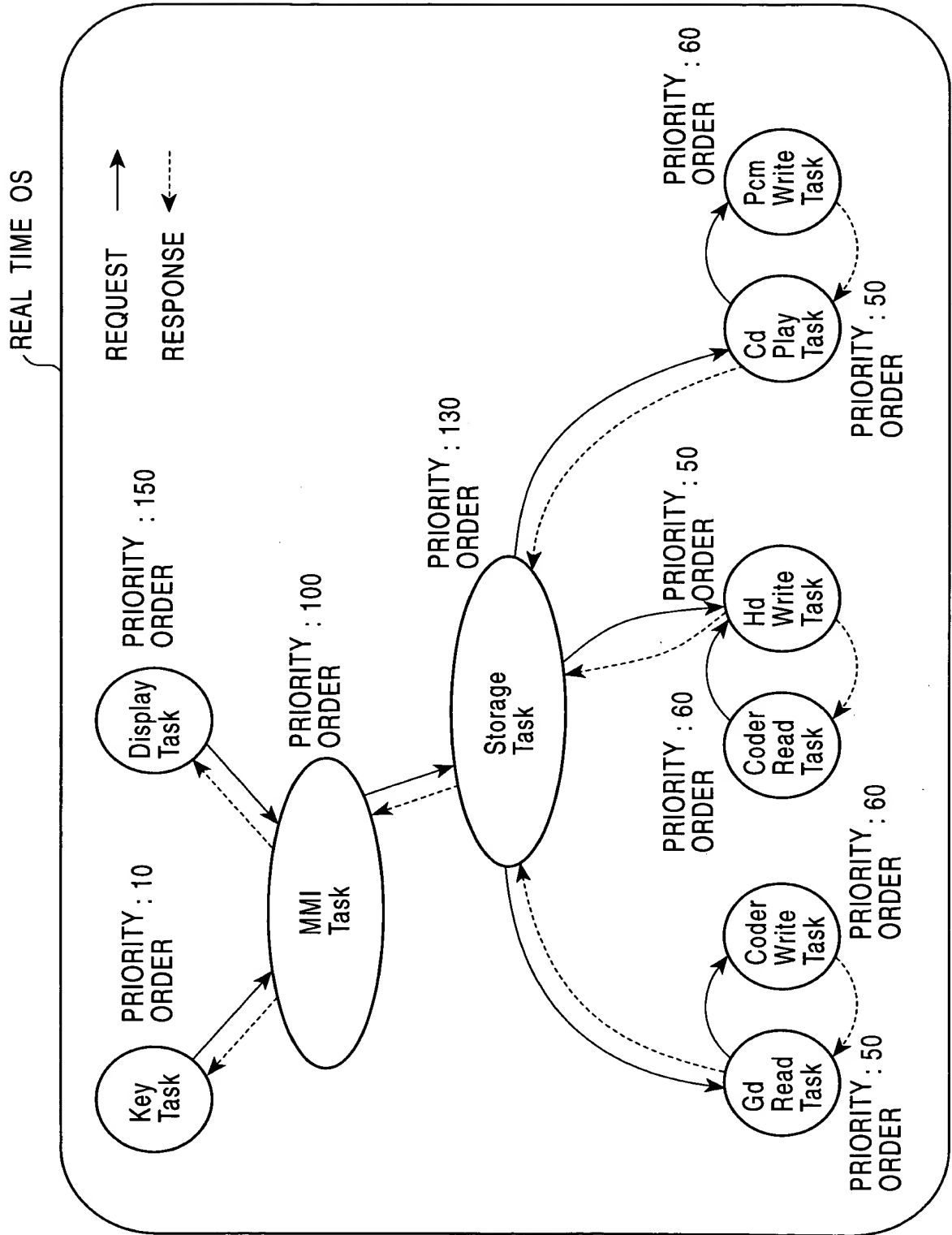


FIG. 35

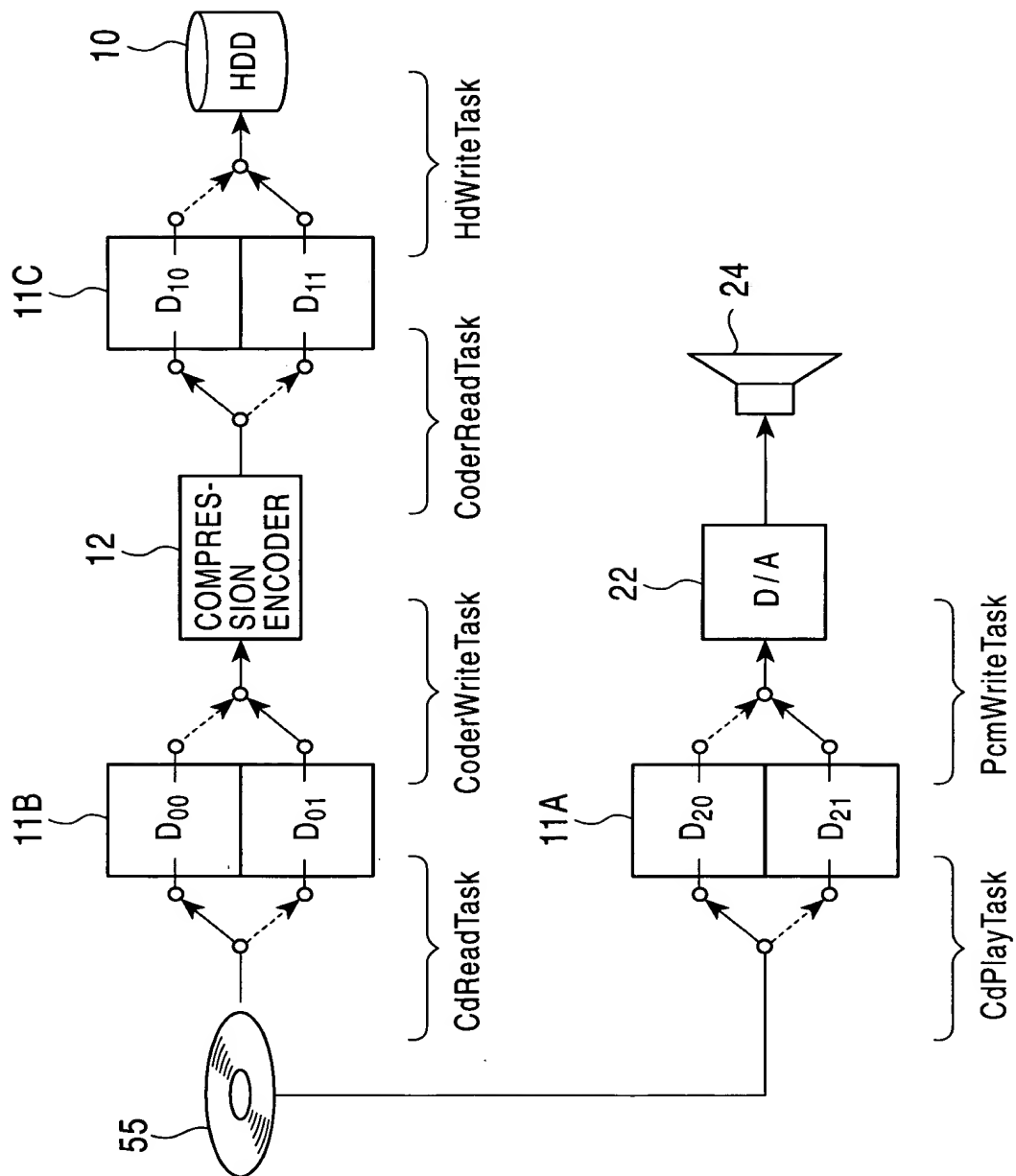
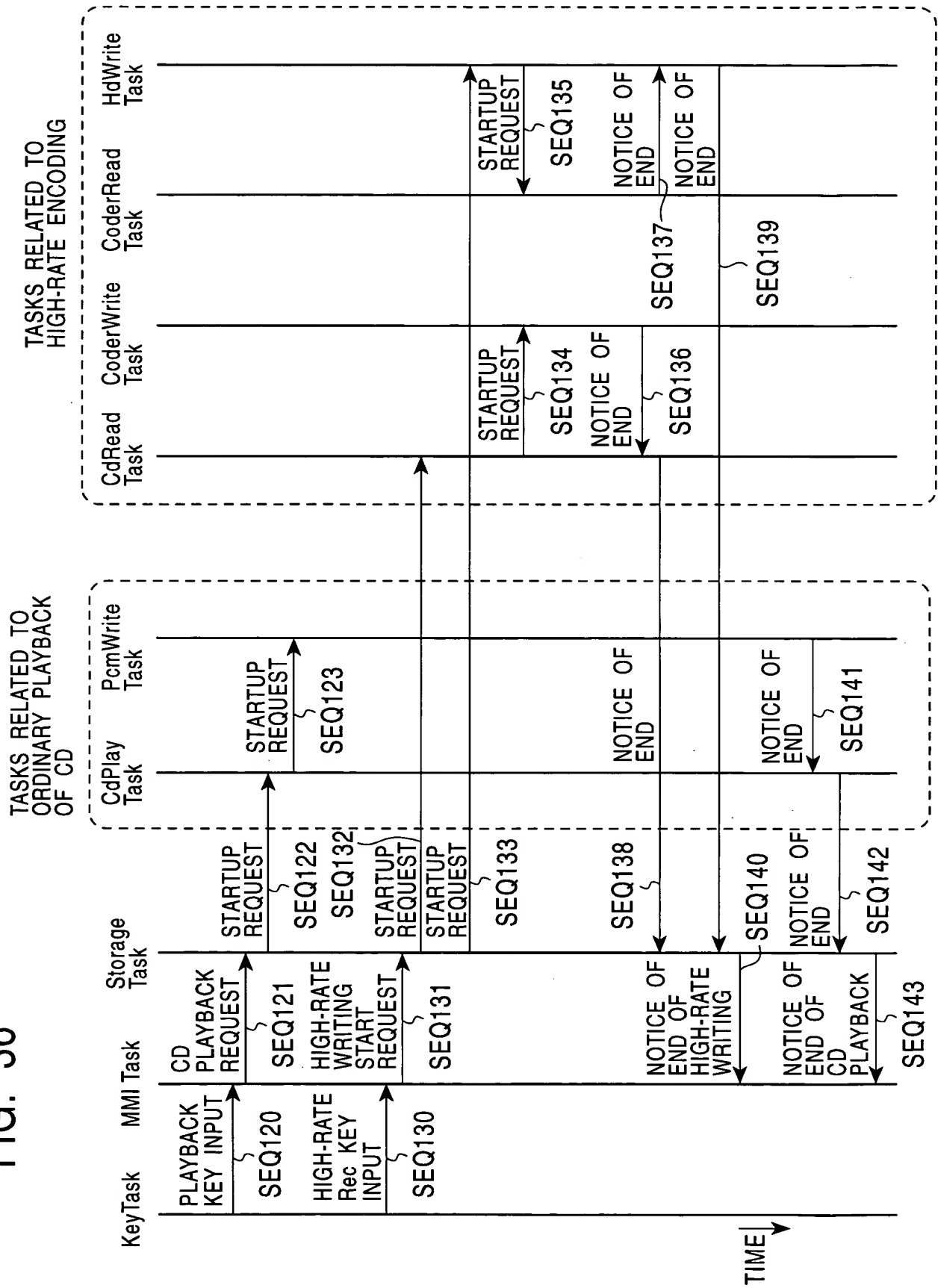


FIG. 36



09691-10500

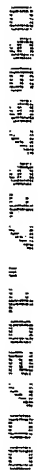
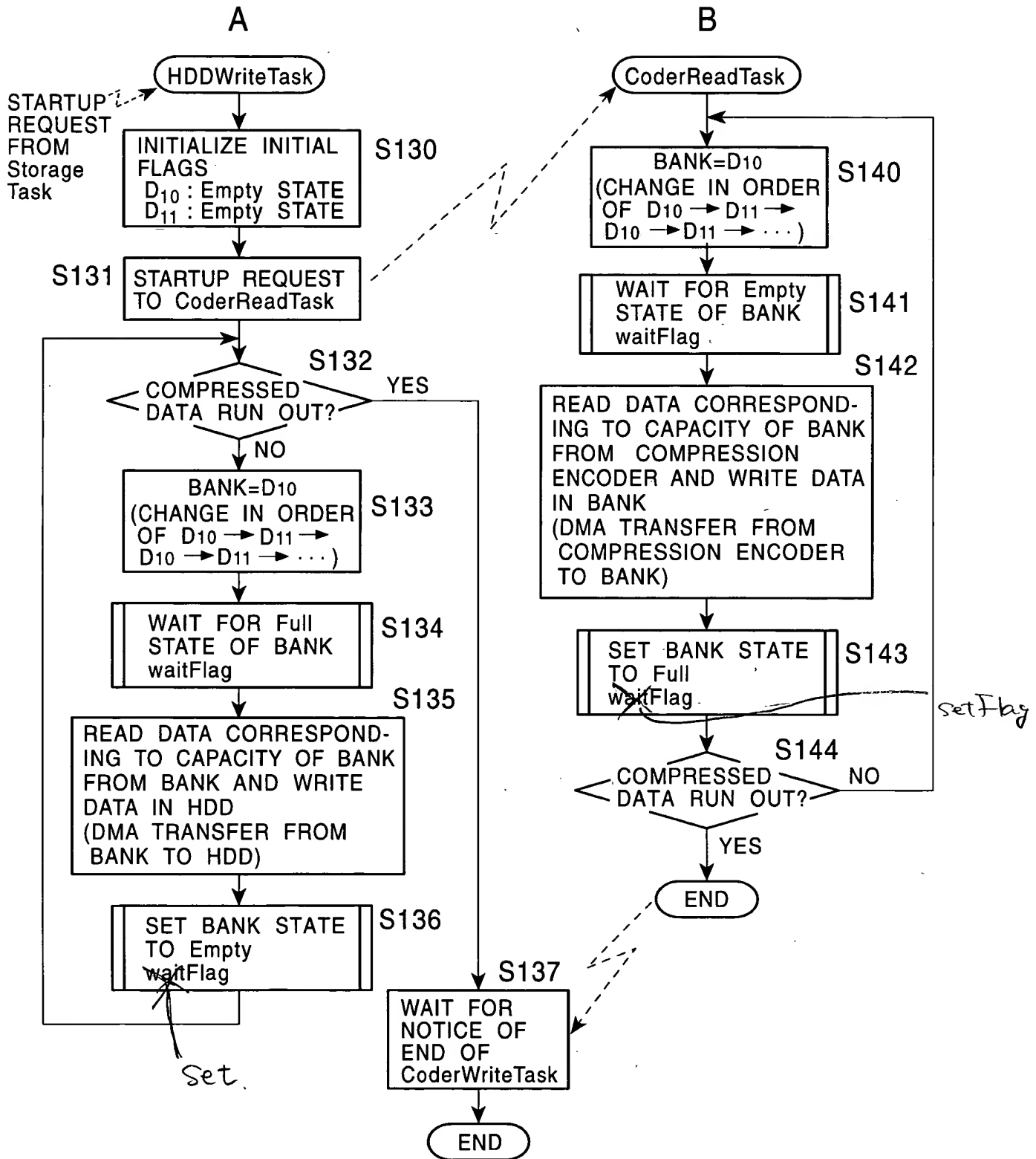
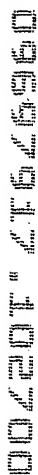


FIG. 38



096701-10



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FIG. 40

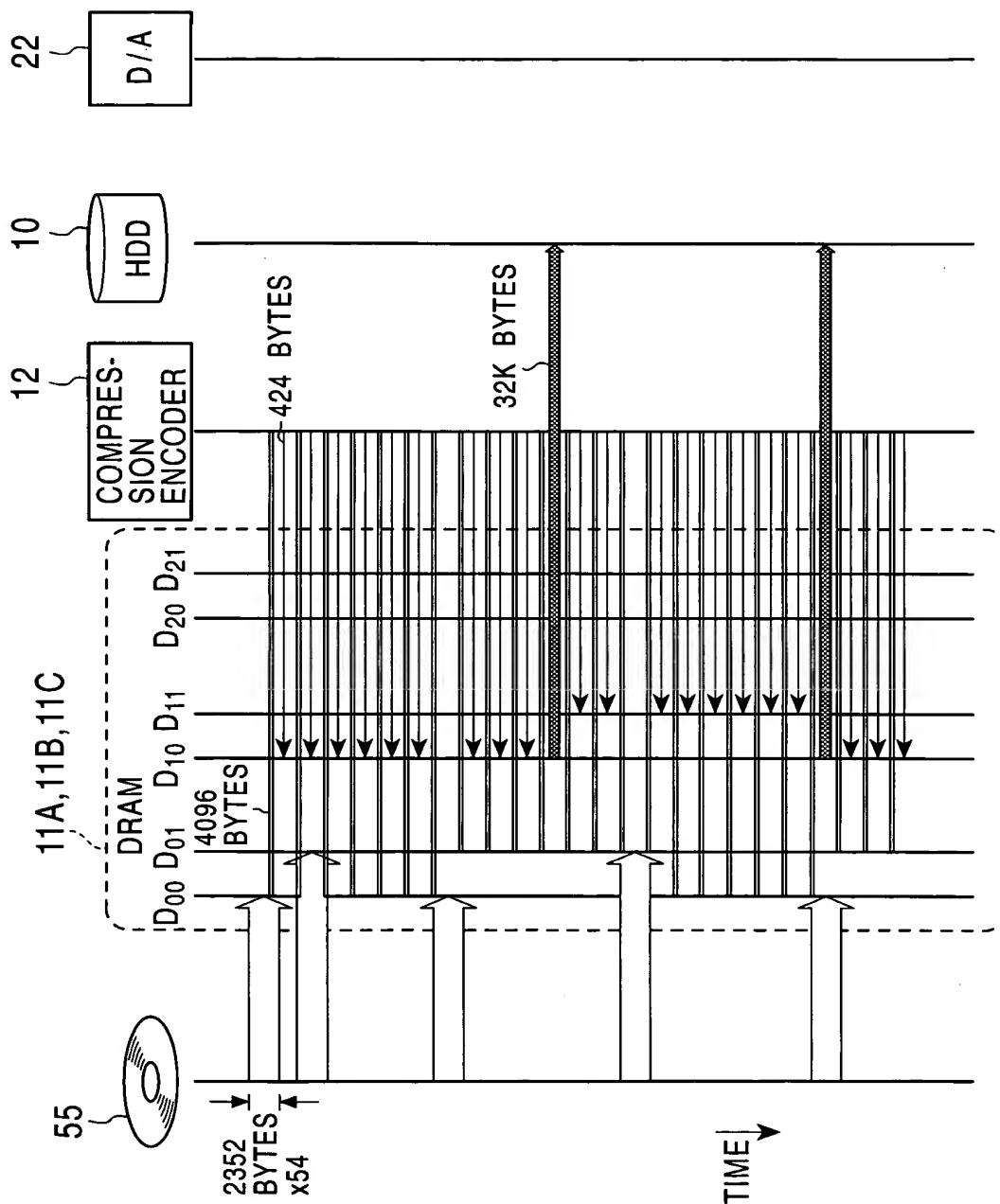


FIG. 40 41

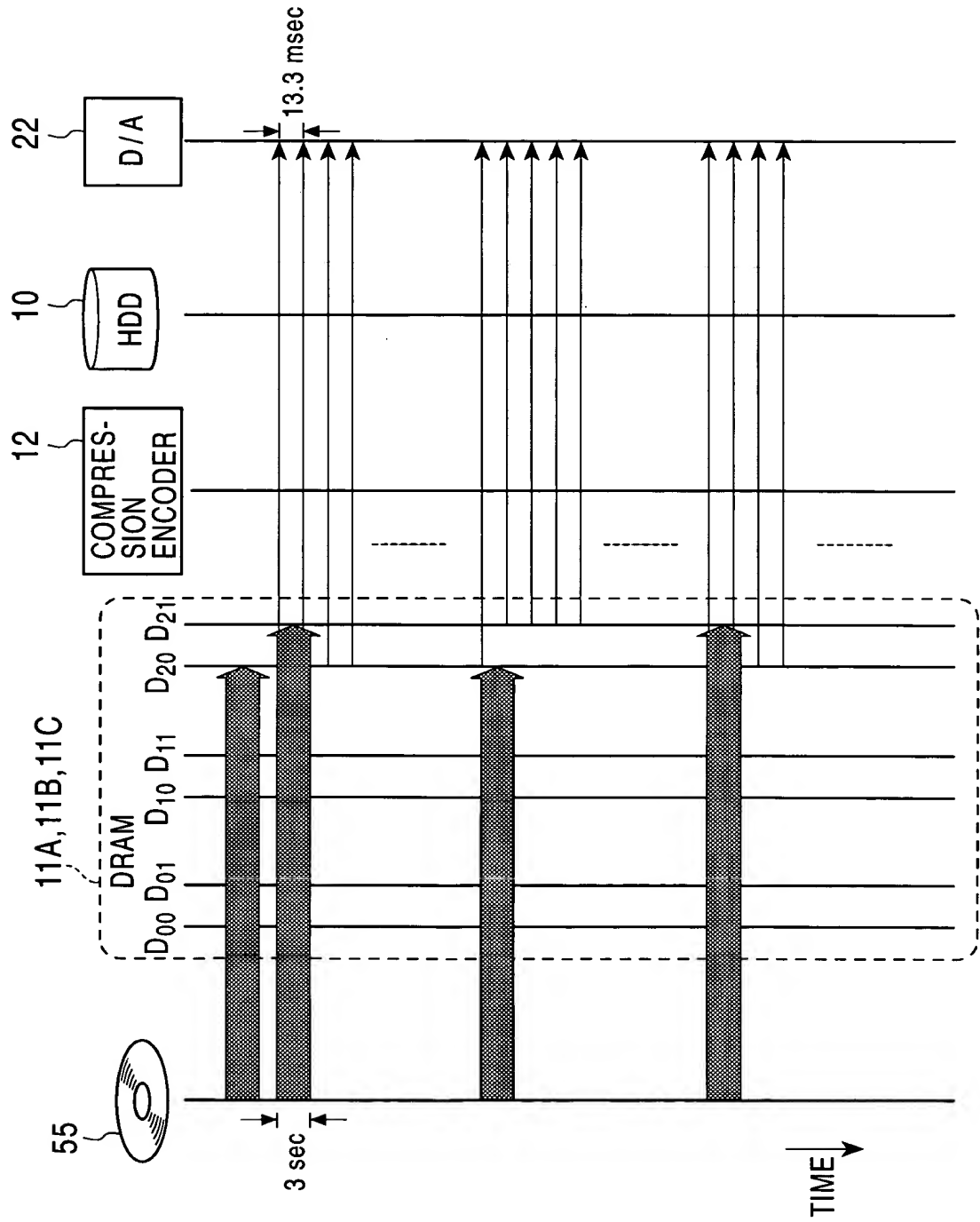
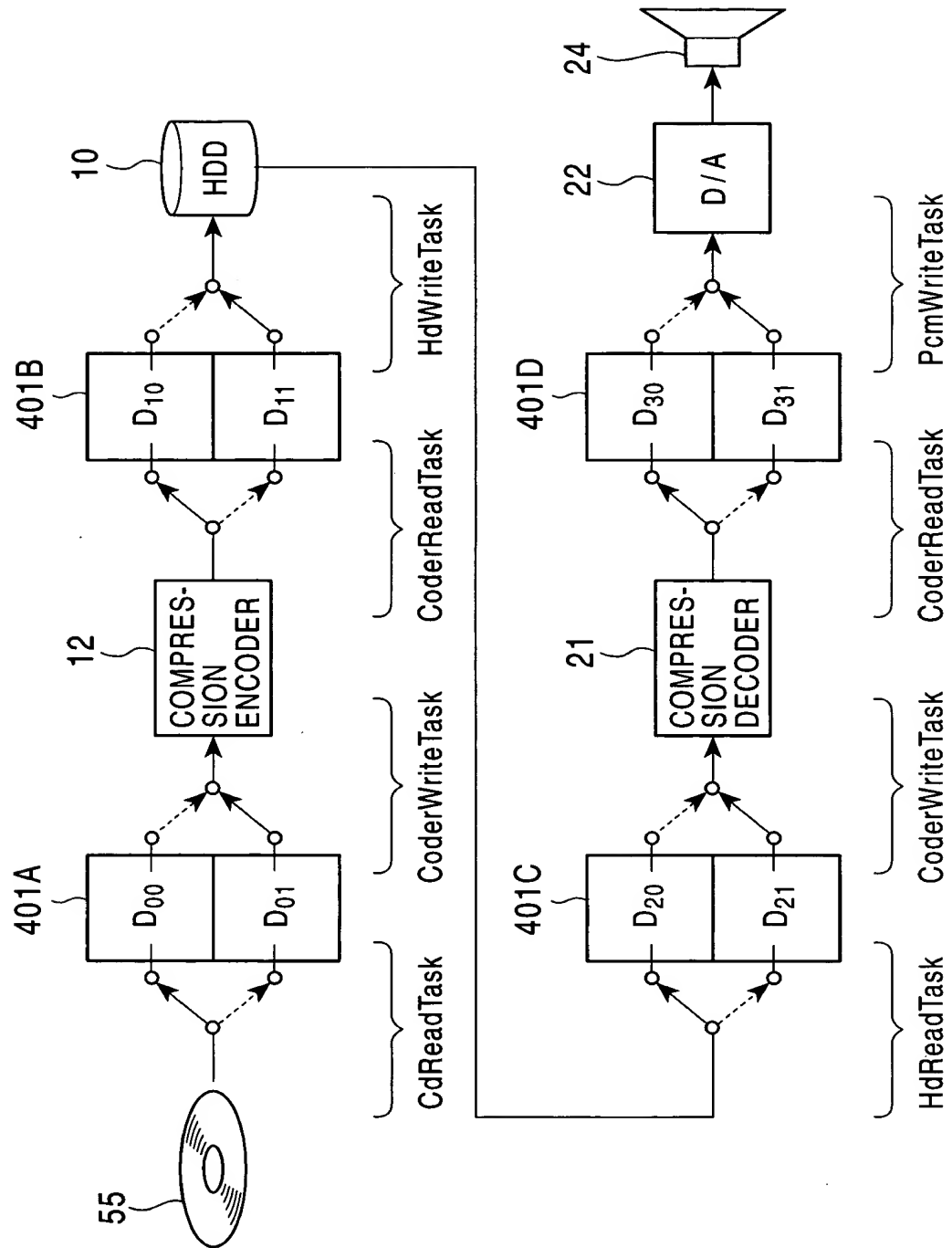


FIG. 42



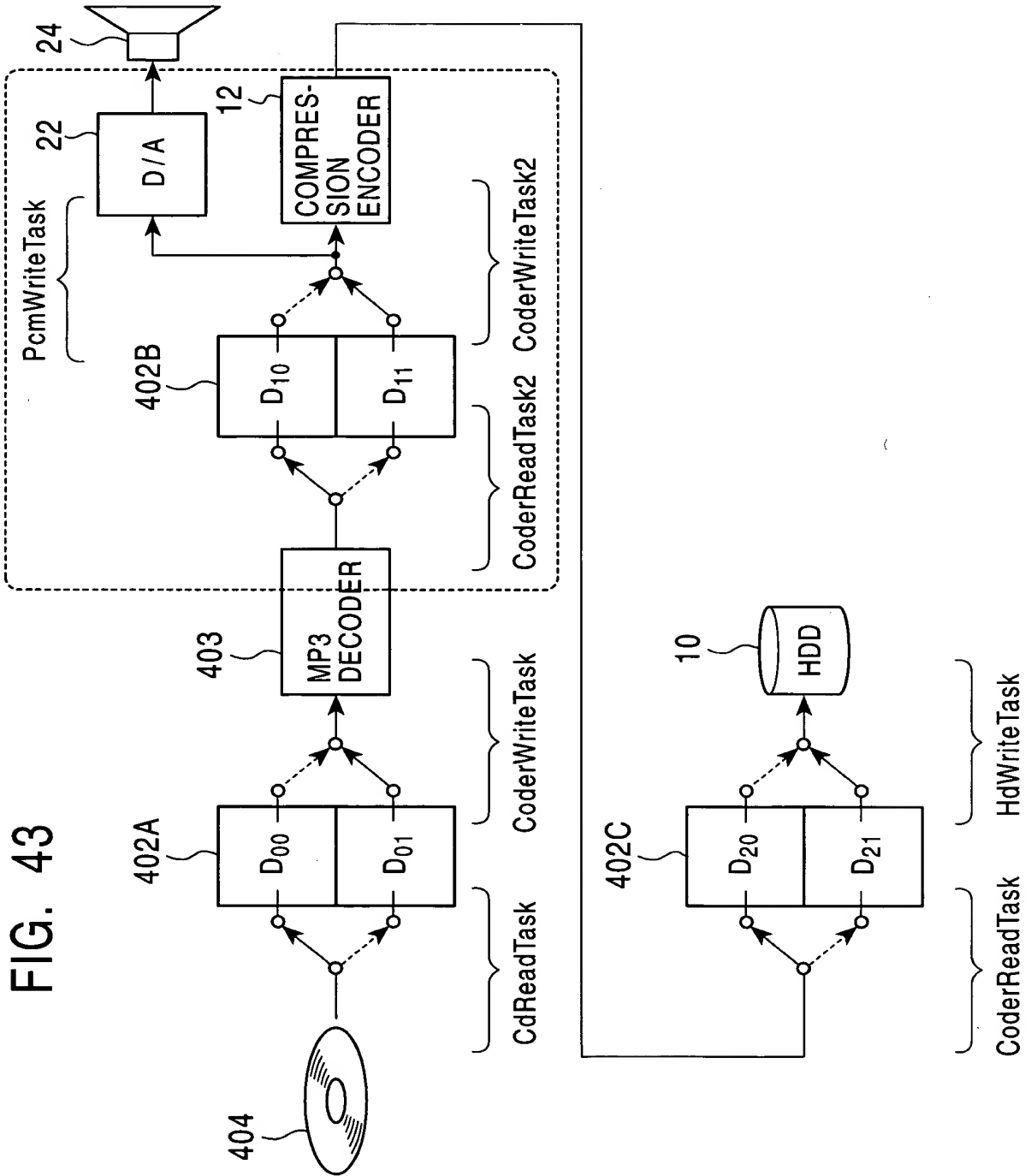


FIG. 44

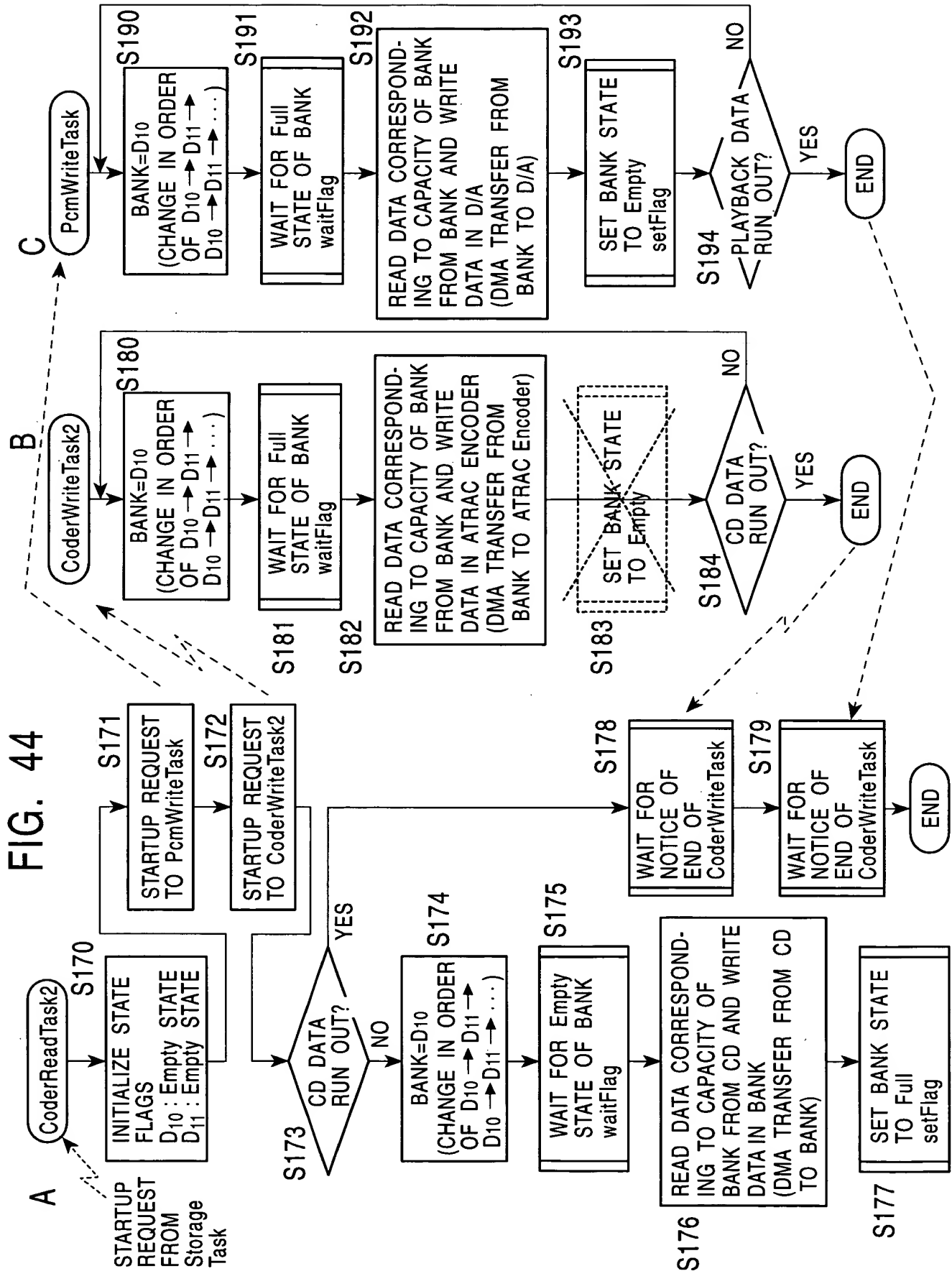


FIG. 45

